

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## HEF4024B

### MSI

## 7-stage binary counter

Product specification  
File under Integrated Circuits, IC04

January 1995

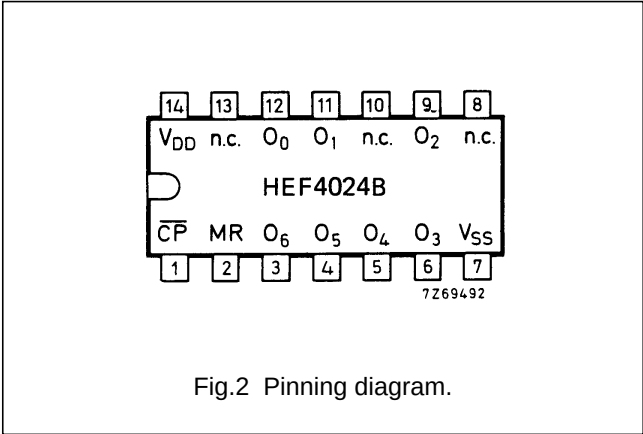
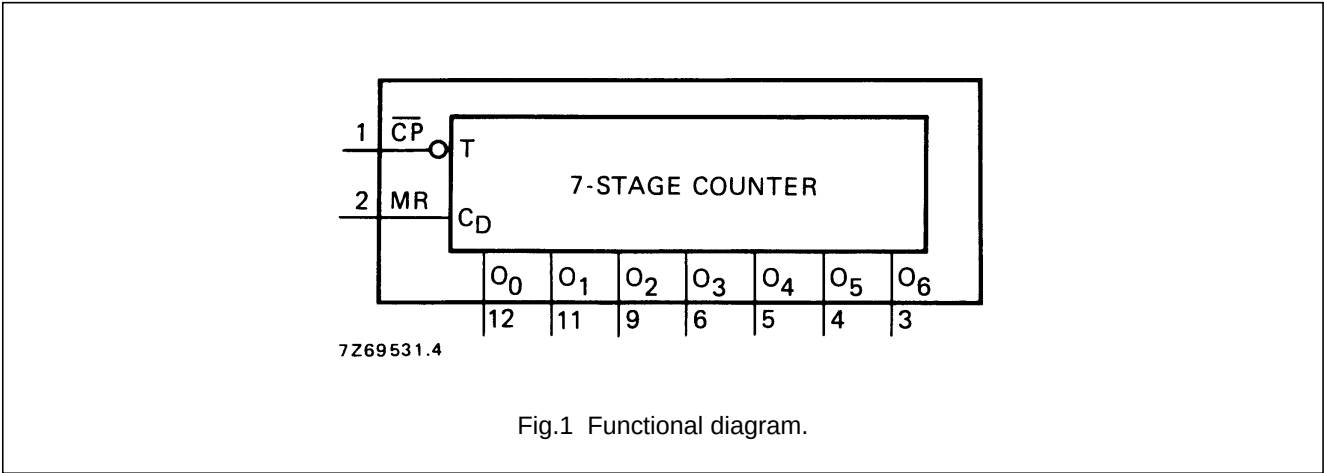
7-stage binary counter

HEF4024B

MSI

DESCRIPTION

The HEF4024B is a 7-stage binary ripple counter with a clock input ( $\overline{CP}$ ), and overriding asynchronous master reset input (MR) and seven fully buffered parallel outputs ( $O_0$  to  $O_6$ ). The counter advances on the HIGH to LOW transition of  $\overline{CP}$ . A HIGH on MR clears all counter stages and forces all outputs LOW, independent of  $\overline{CP}$ . Each counter stage is a static toggle flip-flop.



PINNING

|                 |                                     |
|-----------------|-------------------------------------|
| $\overline{CP}$ | clock input (HIGH to LOW triggered) |
| MR              | master reset input                  |
| $O_0$ to $O_6$  | buffered parallel outputs           |

APPLICATION INFORMATION

Some examples of applications for the HEF4024B are:

- Frequency dividers
- Time delay circuits

FAMILY DATA, I<sub>DD</sub> LIMITS category MSI

See Family Specifications

- HEF4024BP(N): 14-lead DIL; plastic  
(SOT27-1)
- HEF4024BD(F): 14-lead DIL; ceramic (cerdip)  
(SOT73)
- HEF4024BT(D): 14-lead SO; plastic  
(SOT108-1)
- ( ): Package Designator North America

### 7-stage binary counter

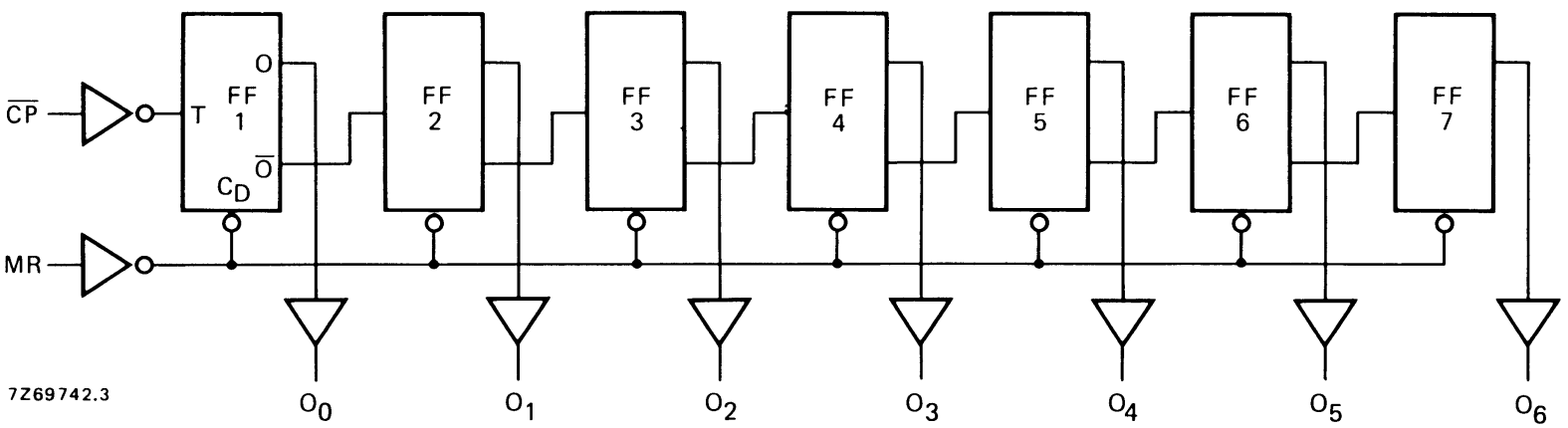
HEF4024B  
MSI

Fig.3 Logic diagram.

## 7-stage binary counter

HEF4024B  
MSI

## AC CHARACTERISTICS

 $V_{SS} = 0$  V;  $T_{amb} = 25$  °C;  $C_L = 50$  pF; input transition times  $\leq 20$  ns; see also waveforms Fig.4

|                                     | V <sub>DD</sub><br>V | SYMBOL            | MIN. | TYP. | MAX. | TYPICAL<br>EXTRAPOLATION<br>FORMULA |                                     |
|-------------------------------------|----------------------|-------------------|------|------|------|-------------------------------------|-------------------------------------|
| Propagation delays                  |                      |                   |      |      |      |                                     |                                     |
| $\overline{CP} \rightarrow O_0$     | 5                    |                   |      | 100  | 200  | ns                                  | 73 ns + (0,55 ns/pF) C <sub>L</sub> |
| HIGH to LOW                         | 10                   | t <sub>PHL</sub>  |      | 40   | 75   | ns                                  | 29 ns + (0,23 ns/pF) C <sub>L</sub> |
|                                     | 15                   |                   |      | 25   | 50   | ns                                  | 17 ns + (0,16 ns/pF) C <sub>L</sub> |
| LOW to HIGH                         | 5                    | t <sub>PLH</sub>  |      | 105  | 210  | ns                                  | 78 ns + (0,55 ns/pF) C <sub>L</sub> |
|                                     | 10                   |                   |      | 45   | 85   | ns                                  | 34 ns + (0,23 ns/pF) C <sub>L</sub> |
|                                     | 15                   |                   |      | 30   | 60   | ns                                  | 22 ns + (0,16 ns/pF) C <sub>L</sub> |
| O <sub>n</sub> → O <sub>n</sub> + 1 | 5                    |                   |      | 60   | 120  | ns                                  | 33 ns + (0,55 ns/pF) C <sub>L</sub> |
| HIGH to LOW                         | 10                   | t <sub>PHL</sub>  |      | 25   | 50   | ns                                  | 14 ns + (0,23 ns/pF) C <sub>L</sub> |
|                                     | 15                   |                   |      | 20   | 40   | ns                                  | 12 ns + (0,16 ns/pF) C <sub>L</sub> |
| LOW to HIGH                         | 5                    | t <sub>PLH</sub>  |      | 50   | 100  | ns                                  | 23 ns + (0,55 ns/pF) C <sub>L</sub> |
|                                     | 10                   |                   |      | 20   | 40   | ns                                  | 9 ns + (0,23 ns/pF) C <sub>L</sub>  |
|                                     | 15                   |                   |      | 15   | 30   | ns                                  | 7 ns + (0,16 ns/pF) C <sub>L</sub>  |
| MR → O <sub>n</sub>                 | 5                    |                   |      | 120  | 240  | ns                                  | 93 ns + (0,55 ns/pF) C <sub>L</sub> |
| HIGH to LOW                         | 10                   | t <sub>PHL</sub>  |      | 45   | 90   | ns                                  | 34 ns + (0,23 ns/pF) C <sub>L</sub> |
|                                     | 15                   |                   |      | 30   | 60   | ns                                  | 22 ns + (0,16 ns/pF) C <sub>L</sub> |
| Output transition times             | 5                    |                   |      | 60   | 120  | ns                                  | 10 ns + (1,0 ns/pF) C <sub>L</sub>  |
| HIGH to LOW                         | 10                   | t <sub>THL</sub>  |      | 30   | 60   | ns                                  | 9 ns + (0,42 ns/pF) C <sub>L</sub>  |
|                                     | 15                   |                   |      | 20   | 40   | ns                                  | 6 ns + (0,28 ns/pF) C <sub>L</sub>  |
| LOW to HIGH                         | 5                    | t <sub>TLH</sub>  |      | 60   | 120  | ns                                  | 10 ns + (1,0 ns/pF) C <sub>L</sub>  |
|                                     | 10                   |                   |      | 30   | 60   | ns                                  | 9 ns + (0,42 ns/pF) C <sub>L</sub>  |
|                                     | 15                   |                   |      | 20   | 40   | ns                                  | 6 ns + (0,28 ns/pF) C <sub>L</sub>  |
| Minimum clock<br>pulse width; HIGH  | 5                    |                   | 60   | 30   |      | ns                                  |                                     |
|                                     | 10                   | t <sub>WCPH</sub> | 30   | 15   |      | ns                                  |                                     |
|                                     | 15                   |                   | 20   | 10   |      | ns                                  |                                     |
| Minimum MR<br>pulse width; HIGH     | 5                    |                   | 80   | 40   |      | ns                                  |                                     |
|                                     | 10                   | t <sub>WMRH</sub> | 35   | 20   |      | ns                                  |                                     |
|                                     | 15                   |                   | 25   | 15   |      | ns                                  |                                     |
| Recovery time<br>for MR             | 5                    |                   | 20   | 10   |      | ns                                  |                                     |
|                                     | 10                   | t <sub>RMR</sub>  | 15   | 5    |      | ns                                  |                                     |
|                                     | 15                   |                   | 15   | 5    |      | ns                                  |                                     |
| Maximum clock<br>pulse frequency    | 5                    |                   | 5    | 10   |      | MHz                                 |                                     |
|                                     | 10                   | f <sub>max</sub>  | 13   | 25   |      | MHz                                 |                                     |
|                                     | 15                   |                   | 18   | 35   |      | MHz                                 |                                     |

7-stage binary counter

HEF4024B  
MSI

|                                                 | $V_{DD}$<br>V | TYPICAL FORMULA FOR P (μW)                  |                                                                                                                                                                  |
|-------------------------------------------------|---------------|---------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Dynamic power<br>dissipation per<br>package (P) | 5             | $500 f_i + \sum (f_o C_L) \times V_{DD}^2$  | where<br>$f_i$ = input freq. (MHz)<br>$f_o$ = output freq. (MHz)<br>$C_L$ = load cap. (pF)<br>$\sum (f_o C_L)$ = sum of outputs<br>$V_{DD}$ = supply voltage (V) |
|                                                 | 10            | $2100 f_i + \sum (f_o C_L) \times V_{DD}^2$ |                                                                                                                                                                  |
|                                                 | 15            | $5200 f_i + \sum (f_o C_L) \times V_{DD}^2$ |                                                                                                                                                                  |

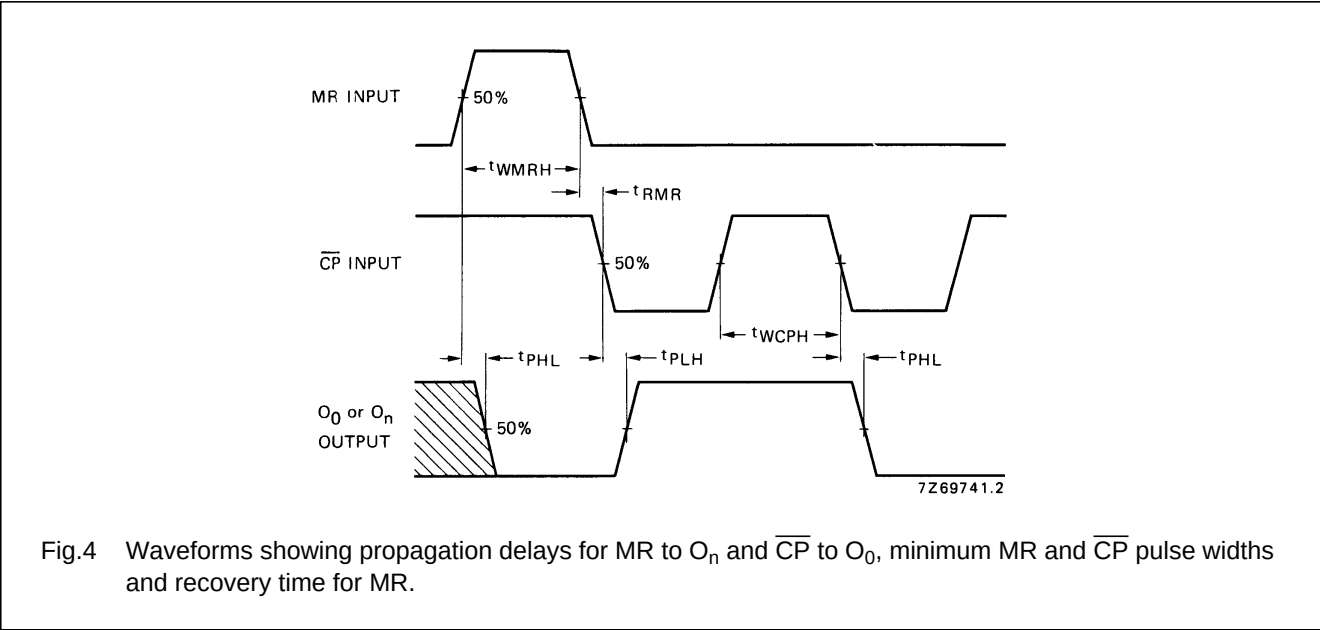


Fig.4 Waveforms showing propagation delays for MR to  $O_n$  and  $\overline{CP}$  to  $O_0$ , minimum MR and  $\overline{CP}$  pulse widths and recovery time for MR.