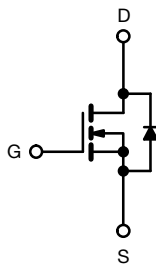


D Series Power MOSFET

TO-220AB


N-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	550	
$R_{DS(on)}$ max. (Ω) at 25 °C	$V_{GS} = 10$ V	0.85
Q_g max. (nC)	30	
Q_{gs} (nC)	4	
Q_{gd} (nC)	7	
Configuration	Single	

FEATURES

- Optimal design
 - Low area specific on-resistance
 - Low input capacitance (C_{iss})
 - Reduced capacitive switching losses
 - High body diode ruggedness
 - Avalanche energy rated (UIS)
- Optimal efficiency and operation
 - Low cost
 - Simple gate drive circuitry
 - Low figure-of-merit (FOM): $R_{on} \times Q_g$
 - Fast switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

APPLICATIONS

- Consumer electronics
 - Displays (LCD or plasma TV)
- Server and telecom power supplies
 - SMPS
- Industrial
 - Welding
 - Induction heating
 - Motor drives
- Battery chargers

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRF840BPbF
Lead (Pb)-free and halogen-free	IRF840BPbF-BE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	500	V
Gate-source Voltage	V_{GS}	± 30	
Gate-source voltage AC ($f > 1$ Hz)		30	
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed drain current ^a	I_{DM}	18	
Linear derating factor		1.25	W/°C
Single pulse avalanche energy ^b	E_{AS}	56	mJ
Maximum power dissipation	P_D	156	W
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Drain-source voltage slope	dV/dt	24	V/ns
Reverse diode dV/dt ^d		0.37	
Soldering recommendations (peak temperature) ^c	For 10 s	300	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 2.3$ mH, $R_g = 25$ Ω , $I_{AS} = 7$ A
- 1.6 mm from case
- $I_{SD} \leq I_D$, starting $T_J = 25$ °C

**THERMAL RESISTANCE RATINGS**

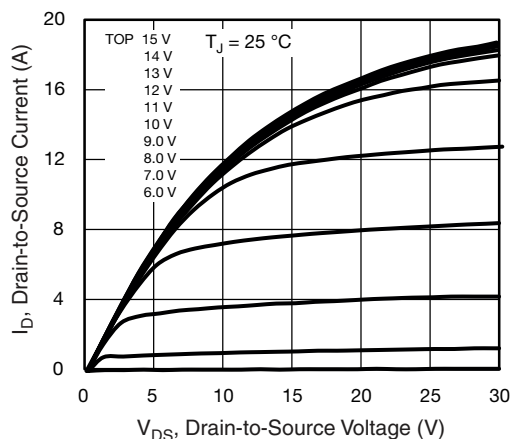
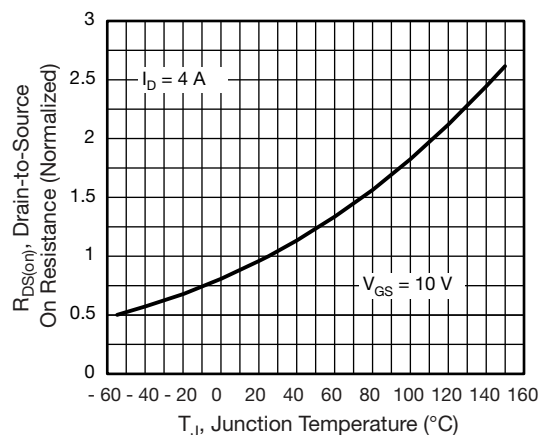
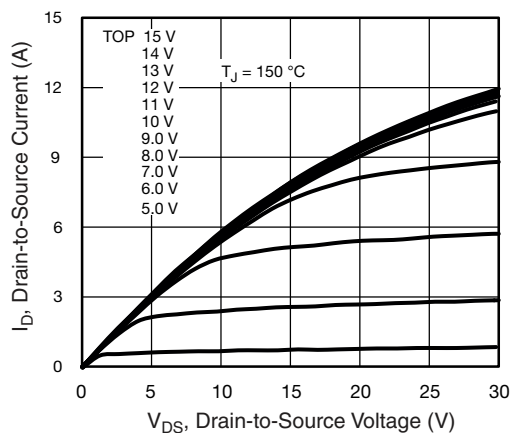
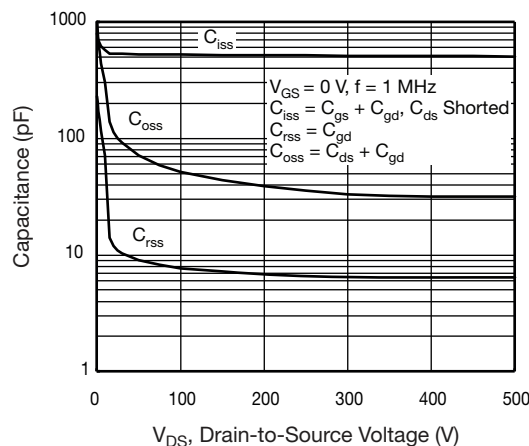
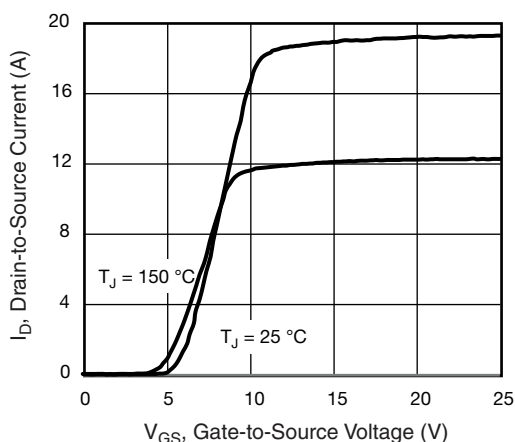
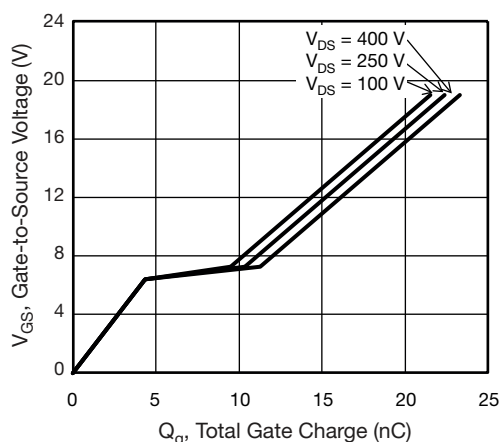
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	0.8	

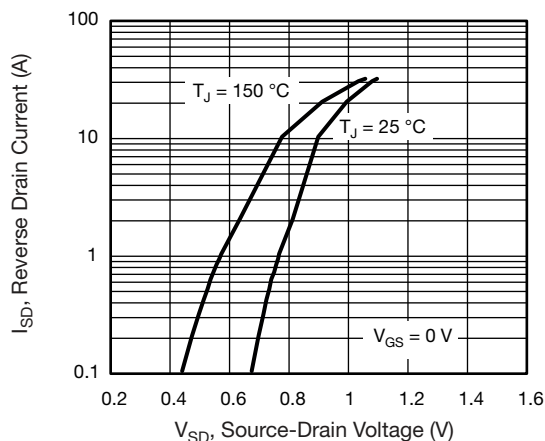
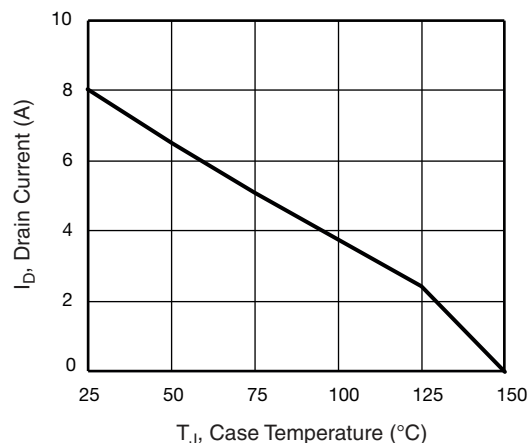
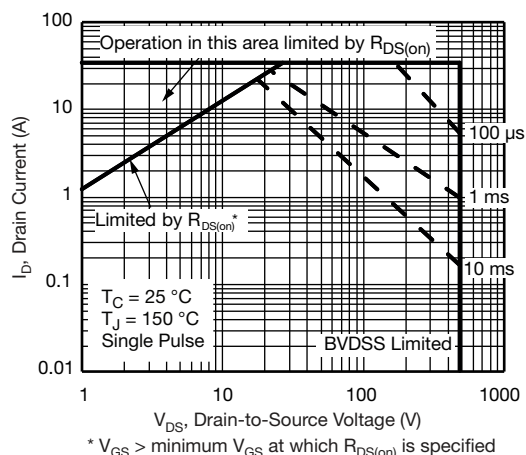
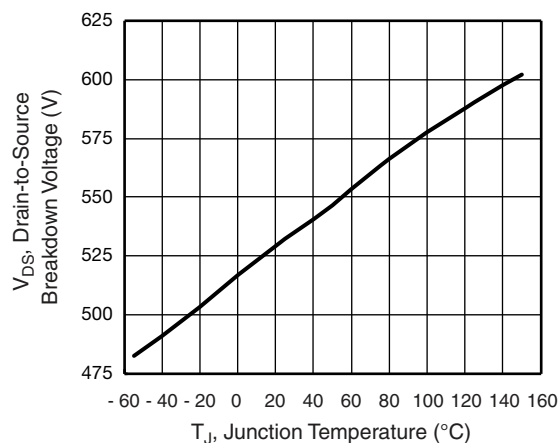
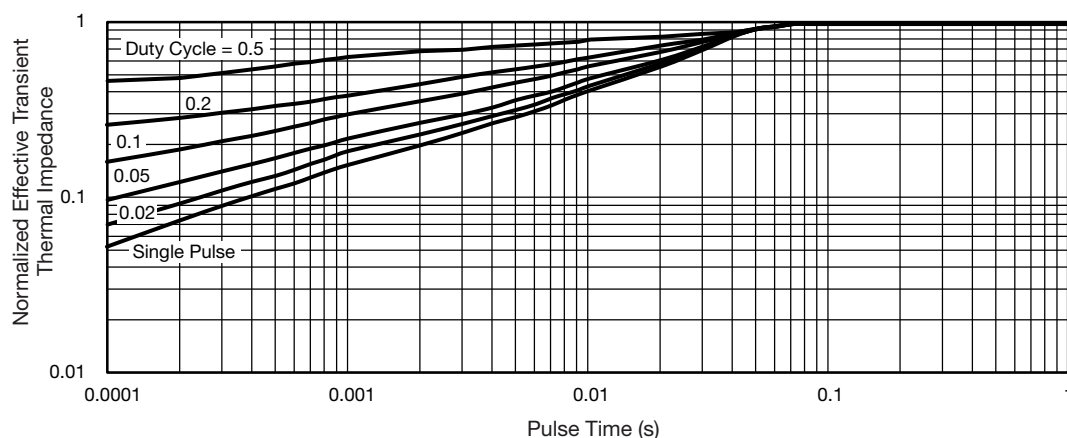
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

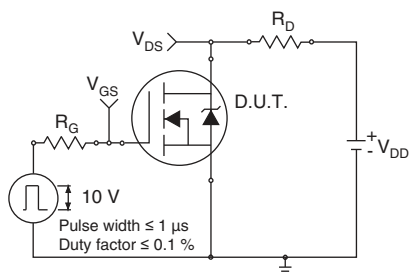
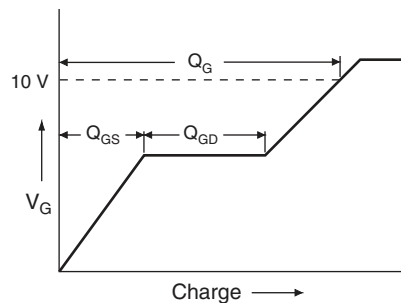
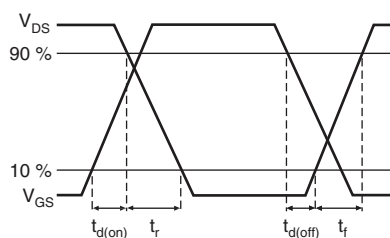
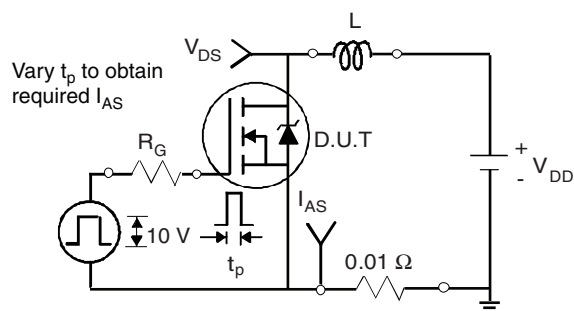
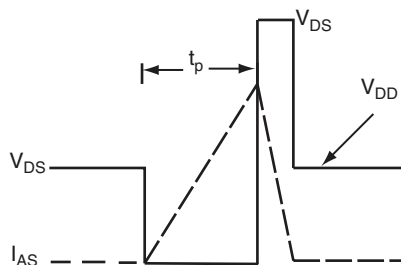
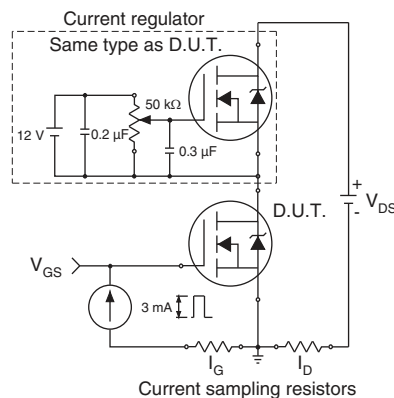
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	500	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 250\text{ }\mu\text{A}$	-	0.58	-	V/ $^{\circ}\text{C}$
Gate-source threshold voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	-	5	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 500\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 400\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$	-	-	10	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 4\text{ A}$	-	0.70	0.85	Ω
Forward transconductance ^a	g_{fs}	$V_{DS} = 20\text{ V}$, $I_D = 4\text{ A}$	-	3	-	S
Dynamic						
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$	-	527	-	pF
Output capacitance	C_{oss}		-	52	-	
Reverse transfer capacitance	C_{rss}		-	8	-	
Effective output capacitance, energy related ^b	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 400\text{ V}$, $V_{GS} = 0\text{ V}$	-	46	-	
Effective output capacitance, time related ^c	$C_{o(tr)}$		-	64	-	
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$, $I_D = 4\text{ A}$, $V_{DS} = 400\text{ V}$	-	15	30	nC
Gate-source charge	Q_{gs}		-	4	-	
Gate-drain charge	Q_{gd}		-	7	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 400\text{ V}$, $I_D = 4\text{ A}$, $R_g = 9.1\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	13	26	ns
Rise time	t_r		-	16	32	
Turn-off delay time	$t_{d(off)}$		-	17	34	
Fall time	t_f		-	11	22	
Gate input resistance	R_g	$f = 1\text{ MHz}$, open drain	-	1.8	-	Ω
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	8	A
Pulsed diode forward current	I_{SM}		-	-	32	
Diode forward voltage	V_{SD}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_S = 4\text{ A}$, $V_{GS} = 0\text{ V}$	-	-	1.2	V
Reverse recovery time	t_{rr}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_F = I_S = 4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_R = 20\text{ V}$	-	308	-	ns
Reverse recovery charge	Q_{rr}		-	1.8	-	μC
Reverse recovery current	I_{RRM}		-	11	-	A

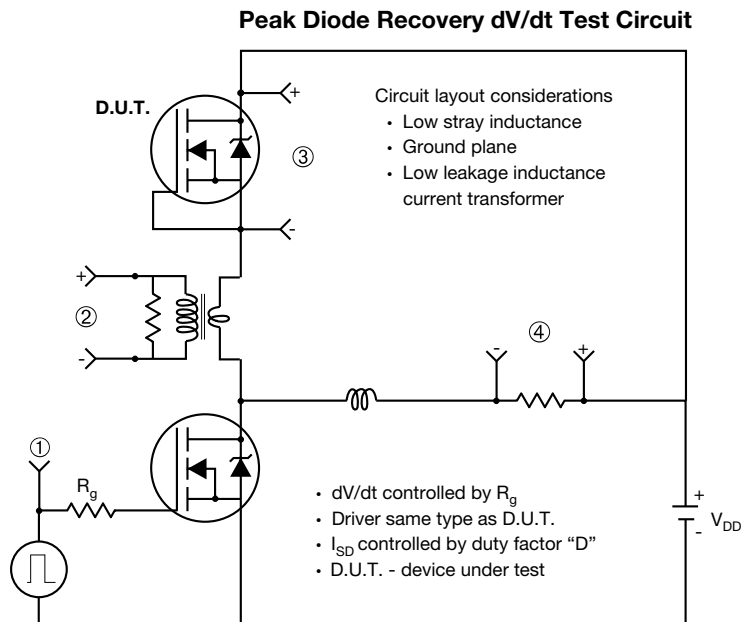
Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature
- b. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
- c. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage


Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Maximum Safe Operating Area

Fig. 10 - Typical Drain-to-Source Voltage vs. Temperature

Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case


Fig. 12 - Switching Time Test Circuit

Fig. 16 - Basic Gate Charge Waveform

Fig. 13 - Switching Time Waveforms

Fig. 14 - Unclamped Inductive Test Circuit

Fig. 15 - Unclamped Inductive Waveforms

Fig. 17 - Gate Charge Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 18 - For N-Channel

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TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
$\varnothing P$	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: E21-0621-Rev. D, 04-Nov-2021
DWG: 6031

Note

- M^* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



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